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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,650	03/01/2004	Harinath B. Kamepalli	SUN040292	9771

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EXAMINER	
DINH, PAUL	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/790,650	KAMEPALLI ET AL.	
	Examiner	Art Unit	
	Paul Dinh	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/3/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the election with traverse filed on 7/7/05.

The examiner acknowledges:

The election of group I (claims 1-11).

The request that claimed 12-20 be canceled without prejudice.

Although applicants did not address any reasons/grounds/evidences/explanations to support the traverse, the restriction requirement, after being reconsidered, is made final. Furthermore, the non-elected claims 12-20 have been cancel per above-mentioned request; no further discussion regarding restriction is necessary.

Claims 1-11 are pending.

Claim Objections

Claims 1 and 8 are objected to because "the contents" and "said output pins" in claim 1 and "the maximum sequential depth" in claim 8 lack antecedent basis.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Rajski et Al (US patent application Publication No. 2002/0053057)

(Claim 1)

For each representation of a circuit design, loading each scannable state element With a symbolic expression (fig 5-7, 11) that characterizes a logical location of said scannable element in the circuit design; and

For each representation of the circuit design, performing a scan shift operation to Verify the contents of each scannable state-element at said scan-out and output pins of the design (fig 2-11).

(Claims 7-8) wherein said loading of each scannable state element with a symbolic expression comprises simulating (abstract, fig 5-6) said circuit design in a functional mode for a first minimum threshold number of cycles by applying symbolic expressions to at least a first input for said circuit design, wherein said first minimum threshold number comprises the maximum sequential depth of all scannable state-elements on all paths from all primary inputs in said circuit design (fig 4-10, para 0048-0051).

(Claims 9-10) wherein said loading and performing steps are implemented with a symbolic simulator to check scan chain equivalency with respect to complete scan chain connectivity from primary input to primary output, logical location of all scannable state elements, scan chain length and scan chain order (fig 4-11); to obtain complete coverage (fig 4-11).

(Claim 11) simulating a sequence of scan clocks equal to a multiple of the number of scannable state-elements in the circuit design (fig 4-11).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a), which forms the basis for all obviousness rejections, set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski Et al (US patent application Publication No. 2002/0053057) in view of Cooke (US patent application Publication No. 2002/0073380)

Rajski discloses substantially all the elements in the claims except behavioral/ transistor/switch levels, RTL/schematic model/netlist.

Cooke discloses behavioral/ transistor/switch levels, RTL model/netlist in paragraphs 9-10, 35, 82, 117-118, 123, 412-413, 435-436, 614, 655, 703, 756-757, 790-797)

It would have been obvious to one of ordinary skill in the art at the time of the invention to use behavioral/ transistor/switch levels, RTL/schematic model/netlist because these elements are regular elements for design/test/verification including scan design/test/verification.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rajski

Et al (US patent application Publication No. 2002/0053057) in view of Lam et al (USP 5084824)

Rajski discloses substantially all the elements in claim 6 except SPICE level netlist and gate level description.

Lam discloses SPICE level netlist and gate level description in col 5-8, 11-14

It would have been obvious to one of ordinary skill in the art at the time of the invention to use SPICE level netlist and gate level description because these elements are known in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Dinh whose telephone number is 571-272-1890. The examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Dinh
Patent Examiner